Exhibit

48C512/48C1024
512K/1024K FLASH™ EEPROM

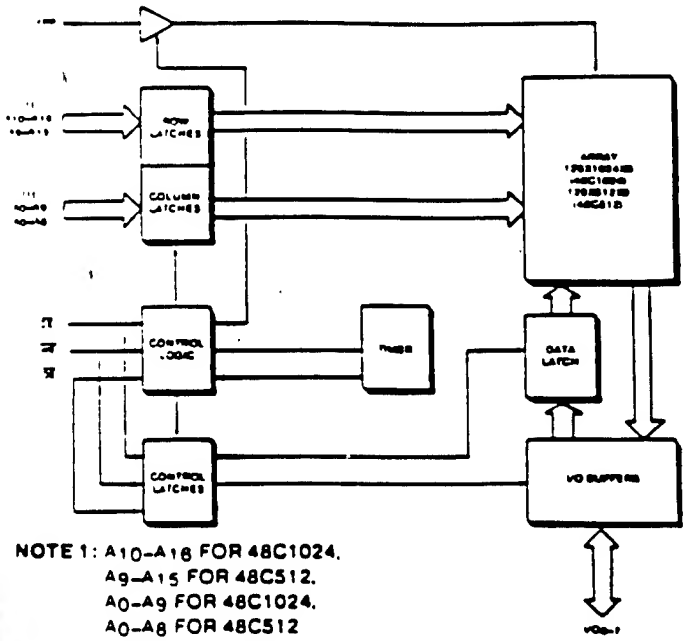
ADVANCE DATA SHEET

July 1987

Features

- 64K/128K Byte Writable Non-Volatile Memory
- Low Power CMOS Process
- Electrical Chip and Block Erase
  - 7.5 Second Maximum Erase Time
- Electrical Byte Write
  - 1 ms. Maximum, 500 µs typical
- Input Latches for Writing and Erasing
- Fast Read Access Time
- Single High Voltage for Writing and Erasing
- Flash™ EEPROM Cell Technology
- Ideal for Low-Cost Program and Data Storage
  - Minimum 100 Cycle Endurance
  - Optional 1000 Cycle Endurance Screening
  - Minimum 10 Year Data Retention
- 5V ± 10% V_{CC}, 0°C to +70°C Temperature Range
- Silicon Signature™ and DITrace™
- Jedec Standard Byte Wide Pinout
  - 32 Pin D.I.P.
  - 32 Pin J-Bend Plastic Leaded Chip Carrier

Block Diagram



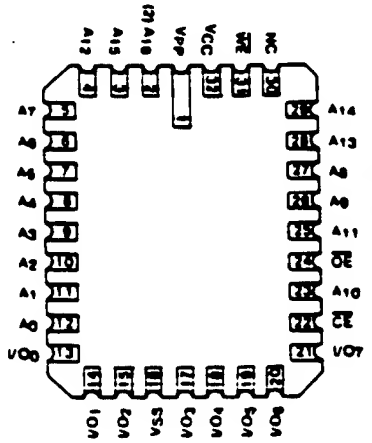
NOTE 1: A_{10}–A_{16} FOR 48C1024,
A_9–A_{15} FOR 48C512,
A_0–A_9 FOR 48C1024,
A_0–A_8 FOR 48C512

NOTE 2: PIN 2 IS N.C. ON THE 48C512

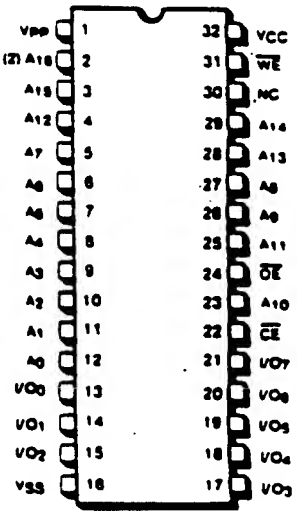
SILICON SIGNATURE™, FLASH™ and DITRACE™ are registered trademarks of SEEQ Technology.

Pin Configuration

TOP VIEW
PLASTIC LEADED CHIP CARRIER



DUAL-IN-LINE
TOP VIEW



Pin Names

A_0-A_8	COLUMN ADDRESS INPUT (48C512)
A_0-A_9	COLUMN ADDRESS INPUT (48C1024)
A_9-A_{15}	ROW ADDRESS INPUT (48C512)
A_{10}-A_{16}	ROW ADDRESS INPUT (48C1024)
$\overline{CE}$	CHIP ENABLE
$\overline{OE}$	OUTPUT ENABLE
$\overline{WE}$	WRITE ENABLE
I/O_{0-7}	DATA INPUT (WRITE)/OUTPUT (READ)
N.C.	NO INTERNAL CONNECTION
V_{PP}	WRITE/ERASE INPUT VOLTAGE

Description

The 48C512 and 48C1024 are 512 Kbit and 1024 Kbit CMOS Flash EEPROMS organized as 64K x 8 and 128K x 8 bits. Built using Seeq's proprietary Flash EEPROM single transistor memory cell, they feature input latches on address and data inputs for both erasing and writing, chip erase and block erase capability and a fast byte write. Endurance, the number of times a byte can be written, is specified as 100 with an optional screen to 1000 cycles.

Read

Reading is accomplished by presenting a valid address with chip enable and output enable at V_{IL}, write enable at V_{IH}, and V_{PP} at any level. See timing waveforms for A.C. parameters.

Erase and Write

Latches on address, data and control inputs permit erasing and writing using normal microprocessor bus timing. Address inputs are latched on the falling edge of write enable or chip enable, whichever is later, while data inputs are latched on the rising edge of write enable or chip enable, whichever is earlier. The write enable input is noise protected: a pulse of less than 20 ns will not initiate a write or erase. In addition, chip enable, output enable and write enable must be in the proper state to initiate a write or erase. Timing diagrams depict write enable controlled writes; the timing also applies to chip enable controlled writes.

Block Erase

Block erase erases all bits in a block of the array to a logical one. It requires that the V_{PP} pin be brought to a high voltage and a write cycle performed. The block to be erased is defined by address inputs A_9 through A_{15} for the 48C512 and A_{10} through A_{16} for the 48C1024. The data inputs must be all ones to begin the erase. Following a write of 'FF', the part will wait for time Tabort to allow aborting the erase by writing again. This permits recovering from an unintentional block erase if, for example, in loading a block of data a byte of 'FF' was written. After the Tabort delay the block erase will begin. The erase is accomplished by following the erase algorithm in figure 2. V_{PP} can be brought to any TTL level or left at high voltage after the erase.

Chip Erase

Chip erase changes all bits in the memory to a logical one. Refer to figure 3 for the chip erase algorithm. V_{PP} can be brought to any TTL level or left at high voltage after the erase.

Block and Chip Erase Algorithm

To reduce the block and chip erase times, a software erase algorithm is used. Refer to figures 2 and 3 for the block erase and chip erase flow charts.

Byte Write

A byte write is used to change any 1 in a byte to a 0. To change a bit in a byte from a 0 to a 1, the byte must be erased first via either block erase or chip erase.

Data are organized in these Flash EEPROMs in a group of bytes called a block. There are 128 blocks in both the 48C512 and the 48C1024. A block, which is 512 bytes in the 48C512 and 1024 bytes in the 48C1024, is conceptually like a sector on a disk drive. Individual bytes must be written as part of a block write algorithm which is detailed in figure 1. This algorithm is designed to minimize the total time to write a block of data.

Blocks are written by applying a high voltage to the V_{PP} pin and writing individual non-FF bytes in sequential order. Each byte write is automatically latched on-chip, so that the user can do a normal microprocessor write cycle and then wait a minimum of t_{WC} ns. for the self-timed write to complete. Each byte write incrementally programs bits that are to become a zero. A write loop has been completed when all non-FF data for all desired blocks have been written. Following each loop, a read-verification is done. If any bytes do not verify, another write loop is performed. When all bytes read correctly, additional loops are performed to insure adequate bit cell margin. The total number of loops will vary by device and depends on temperature; low temperature reduces

the number of loops required. For example, a typical (room temperature) loop count is 4. Blocks need not be written separately; the entire device or any combination of blocks can be written using the write algorithm.

Because bytes can only be written as part of a block write, if data is to be added to a partially written block or one or more bytes in a block must be changed, the contents of the block must first be read into system RAM; the bytes can then be added to the block of data in RAM and the block written using the block write algorithm.

Power Up/Down Protection

These two devices contain a V_{CC} sense circuit which disables internal erase and write operations when V_{CC} is below 3.5 volts. In addition, erases and writes are prevented when any control input (CE, OE, WE) is in the wrong state for writing or erasing (see mode table).

High Voltage Input Protection

The V_{PP} pin is at a high voltage for writing and erasing. There is an absolute maximum specification which must not be exceeded, even briefly, or permanent device damage may result. To minimize switching transients on this pin we recommend using a minimum 0.1 uf decoupling capacitor with good high frequency response connected from V_{PP} to ground at each device. In addition, sufficient bulk capacitance should be provided to minimize V_{PP} voltage sag when a device goes from standby to a write or erase cycle.

Silicon Signature™

A row of fixed ROM is present in the 48C512 and 48C1024 which contains the device's Silicon Signature™. Silicon Signature™ contains data which identifies Seeq as the manufacturer and gives the product code. This allows device programmers to match the programming specification against the product which is to be programmed.

Silicon Signature™ is read by raising address A_9 to 12 ± 0.5 V, and bringing all other address inputs plus chip enable and output enable to V_{IL} with V_{CC} at 5 V. The two Silicon Signature™ bytes are selected by address input A_0. Silicon Signature™ is functional at room temperature only (25 C).

Silicon Signature™ Bytes

	A_0	Data (Hex)
Seeq Code	V_{IL}	94
Product code (48C512)	V_{IH}	1A
Product code (48C1024)	V_{IH}	1C

Mode Selection Table

MODE	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	V_{PP}	A_{9-15} A_{10-15}	A_{0-8} A_{0-9}	D_{0-7}
Read	V_{IL}	V_{IL}	V_{IH}	X	Address	Address	D_{OUT}
Standby	V_{IH}	X	X	X	X	X	HI-Z
Byte write	V_{IL}	V_{IH}	V_{IL}	V_P	Address	Address	D_{IN}
Chip erase select	V_{IL}	V_{IH}	V_{IL}	TTL	X	X	X
Chip erase	V_{IL}	V_{IH}	V_{IL}	V_P	X	X	'FF'
Block erase	V_{IL}	V_{IH}	V_{IL}	V_P	Address	X	'FF'

DC Operating Characteristics

Over the V_{CC} and temperature range

Symbol	Parameter	Limits			Test Condition
		Min.	Max.	Unit	
I_{IH}	Input leakage high		1	µA	$V_{IN} = V_{CC}$
I_{IL}	Input leakage low		−1	µA	$V_{IN} = 0.1$ v
I_{OL}	Output leakage		10	µA	$V_{IN} = V_{CC}$
V_P	Program/erase voltage	11.5	12.5	V	
V_{PP}	V_{PP} voltage during read	0	V_P	V	
I_{PP}	V_P current Standby mode Read mode Byte write Erase		 200 200 40 60	 µA µA mA mA	 $\overline{CE} = V_{IH}$, $V_{PP} = V_P$ $\overline{CE} = V_{IL}$, $V_{PP} = V_P$ $V_{PP} = V_P$ $V_{PP} = V_P$
I_{CC1}	Standby V_{CC} current		100	µA	$\overline{CE} = V_{CC} - .3$
I_{CC2}	Standby V_{CC} current		5	mA	$\overline{CE} = V_{IH}$ min.
I_{CC3}	Active V_{CC} current		60	mA	$\overline{CE} = V_{IL}$
V_{IL}	Input low voltage	−0.3	0.8	V	
V_{IH}	Input high voltage	2.0	$V_{CC}+.3$	V	
V_{OL}	Output low voltage		0.45	V	$I_{OL} = 2.1$ ma
V_{OH1}	Output level (TTL)	2.4		V	$I_{OH} = -400\mu A$
V_{OH2}	Output level (CMOS)	$V_{CC}-.4$		V	$I_{OH} = -100\ \mu A$

AC Test Conditions

Output load: 1 TTL gate and C(load) = 100 pf.
Input rise and fall times: < 20 ns.
Input pulse levels: 0.45 V to 2.4 V
Timing measurement reference level:
Inputs 1 V and 2 V
Outputs 0.8 V and 2 V

NOTE:
In A.C. characteristics, all inputs to the device, e.g., setup time, hold time and cycle time, are tabulated as a minimum time; the user must provide a valid state on that input or wait for the stated minimum time to assure proper operation. All outputs from the device, e.g., access time, erase time, recovery time, are tabulated as a maximum time, the device will perform the operation within the stated time.

Advance Data Sheets contain target product specifications which are subject to change upon device characterization over the full specified temperature range. These specifications may be changed at any time, without notice.

Absolute Maximum Stress Ratings

Temperature:
Storage ..... −65°C to +150°C
Under bias ..... −10°C to +85°C

All inputs except V_{DD} and outputs with Respect to V_{SS} ... +6 V to −0.3 V

V_{DD} pin with respect to V_{SS} ... 14 V

E.S.D. Characteristics

Symbol	Parameter	Value	Test Conditions
V_{ZAP}	E.S.D. Tolerance	>2000 V	MIL-STD 883 Method 3015

Note: Characterization data — not tested.

Recommended Operating Conditions

	48C512/ 48C1024
V_{CC} supply voltage	5V ± 10%
Temperature range	0°C to 70°C (ambient temp.)

Capacitance[1] T_A=25°C, f=1 MHz

Symbol	Parameter	Value	Test Conditions
C_{IN}	Input capacitance	6 pf.	V_{IN} = 0 V
C_{OUT}	Output capacitance	12 pf.	$V_{I/O}$ = 0 V

Note 1: This parameter is only sampled and not 100% tested.

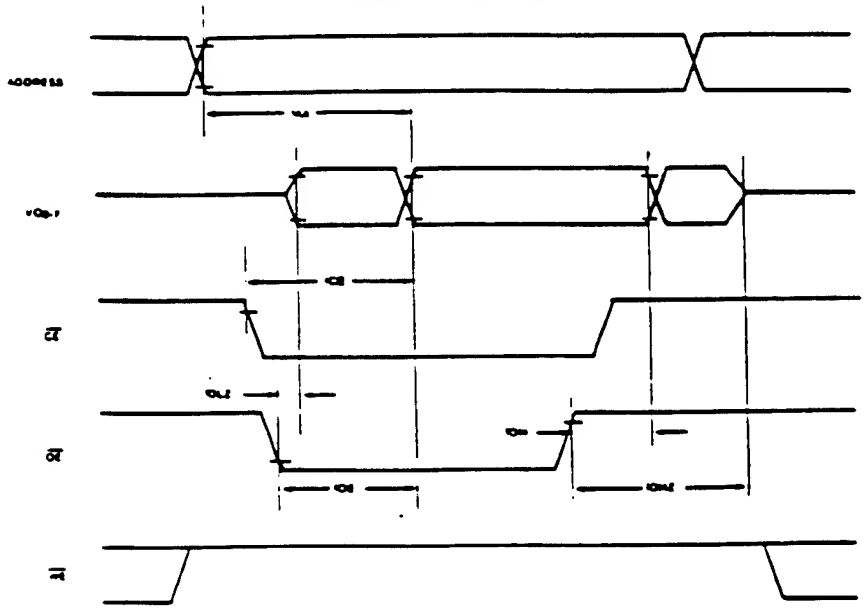
AC Characteristics

(over the V_{CC} and temperature range)

READ

Symbol	Parameter	48CXXXX -200		48CXXXX -250		48CXXXX -300		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{RC}	Read cycle time	200		250		300		ns
t_{AA}	Address to data		200		250		300	ns
t_{CE}	$\overline{CE}$ to data		200		250		300	ns
t_{OE}	$\overline{OE}$ to data		75		100		150	ns
t_{OF}	$\overline{OE}/\overline{CE}$ to data float		50		60		100	ns
t_{OH}	Output hold time	0		0		0		ns

Read Timing



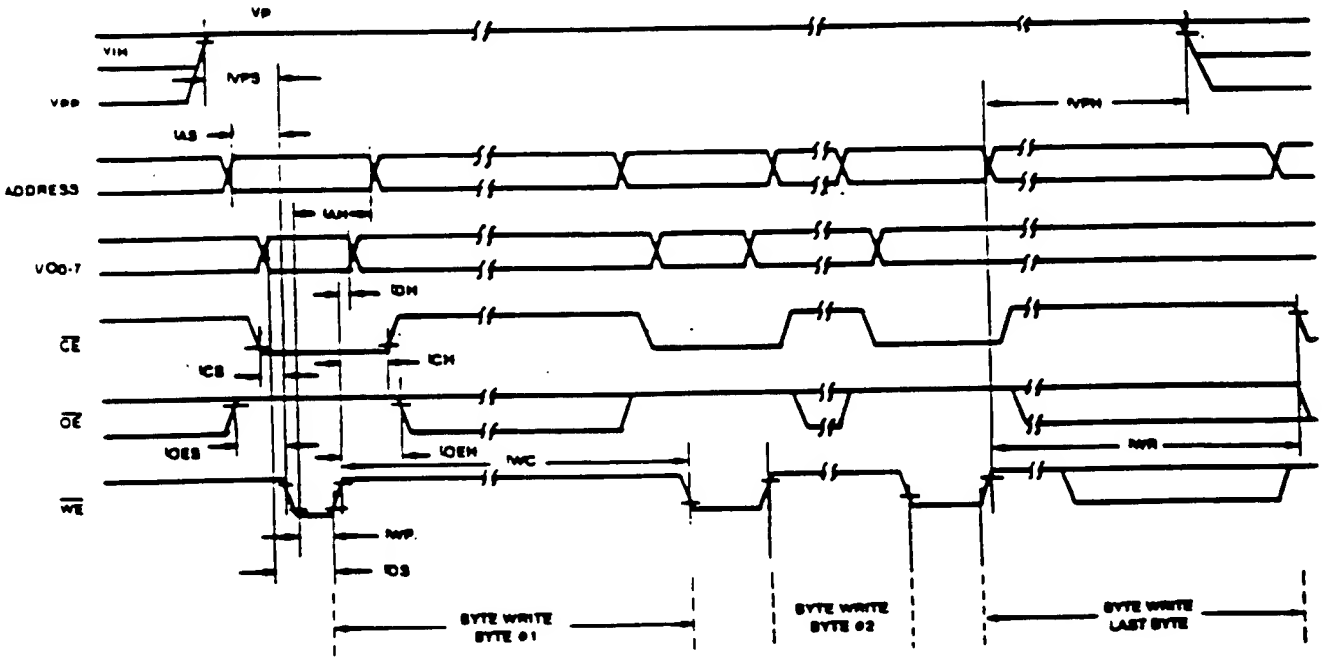
AC Characteristics

(Over the V_{CC} and temperature range)

BYTE WRITE

Symbol	Parameter	48CXXXX -200		48CXXXX -250		48CXXXX -300		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{VPS}	V_{PP} setup time	2		2		2		µs
t_{VPH}	V_{PP} hold time	250		250		250		µs
t_{CS}	$\overline{CE}$ setup time	0		0		0		ns
t_{CH}	$\overline{CE}$ hold time	0		0		0		ns
t_{OES}	$\overline{OE}$ setup time	10		10		10		ns
t_{OEH}	$\overline{OE}$ hold time	10		10		10		ns
t_{AS}	Address setup time	20		20		20		ns
t_{AH}	Address hold time	100		100		100		ns
t_{DS}	Data setup time	50		50		50		ns
t_{DH}	Data hold time	0		0		0		ns
t_{WP}	$\overline{WE}$ pulse width	100		100		100		ns
t_{WC}	Write cycle time	100	150	100	150	100	150	µs
t_{WR}	Write recovery time		1.5		1.5		1.5	ms

Byte Write Timing

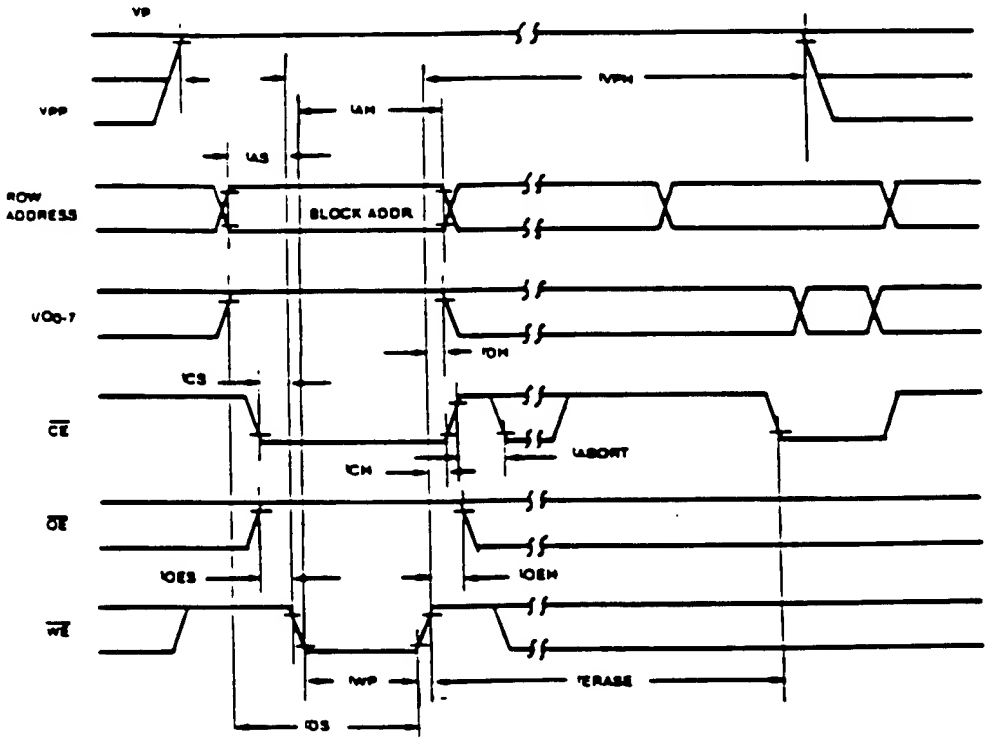


AC Characteristics — BLOCK ERASE

(Over the V_{CC} and temperature range)

Symbol	Parameter	48CXXXX -250		48CXXXX -300		48XXXX -350		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{VPS}	V_{PP} setup time	2		2		2		µs
t_{VPH}	V_{PP} hold time	500		500		500		ms
t_{CS}	$\overline{CE}$ setup time	0		0		0		ns
t_{OES}	$\overline{OE}$ setup time	0		0		0		ns
t_{AS}	Address setup time	20		20		20		ns
t_{AH}	Address hold time	100		100		100		ns
t_{DS}	Data setup time	50		50		50		ns
t_{DH}	Data hold time	0		0		0		ns
t_{WP}	$\overline{WE}$ pulse width	100		100		100		ns
t_{CH}	$\overline{CE}$ hold time	0		0		0		ns
t_{OEH}	$\overline{OE}$ hold time	0		0		0		ns
t_{ERASE}	Block erase time		500		500		500	ms
t_{ABORT}	Block erase delay		250		250		250	µs

Block Erase Timing



AC Characteristics — CHIP ERASE

(Over the V_{CC} and temperature range)

Symbol	Parameter	48CXXXX -200		48CXXXX -250		48CXXXX -300		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{VPS}	V_{PP} setup time	2		2		2		µs
t_{VPH}	V_{PP} hold time	500		500		500		ms
t_{CS}	$\overline{CE}$ setup time	0		0		0		ns
t_{OES}	$\overline{OE}$ setup time	0		0		0		ns
t_{DS}	Data setup time	50		50		50		ns
t_{DH}	Data hold time	0		0		0		ns
t_{WP}	$\overline{WE}$ pulse width	100		100		100		ns
t_{CH}	$\overline{CE}$ hold time	0		0		0		ns
t_{OEH}	$\overline{OE}$ hold time	0		0		0		ns
t_{ERASE}	Chip erase time		500		500		500	ms

Chip Erase Timing

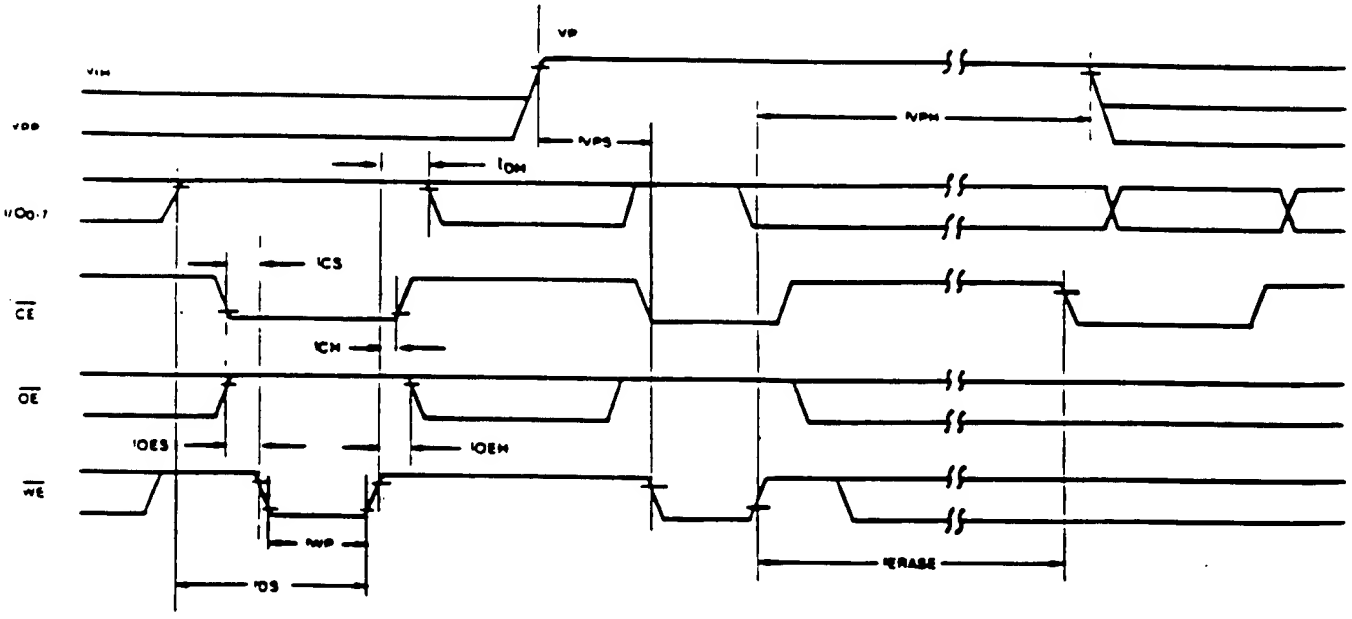


FIGURE 1
48C512/1024 WRITE ALGORITHM

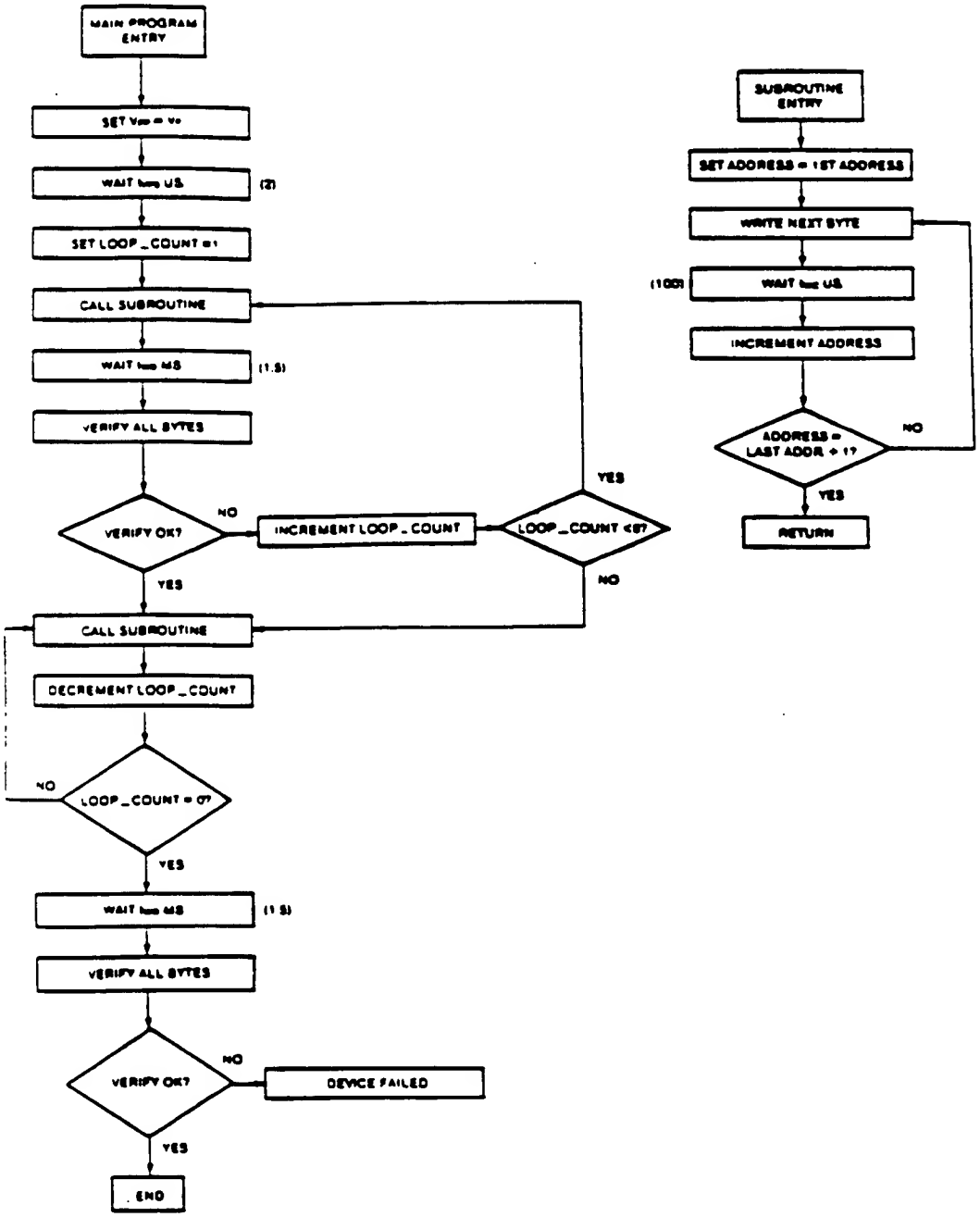


FIGURE 2
48C512/1024

BLOCK ERASE ALGORITHM

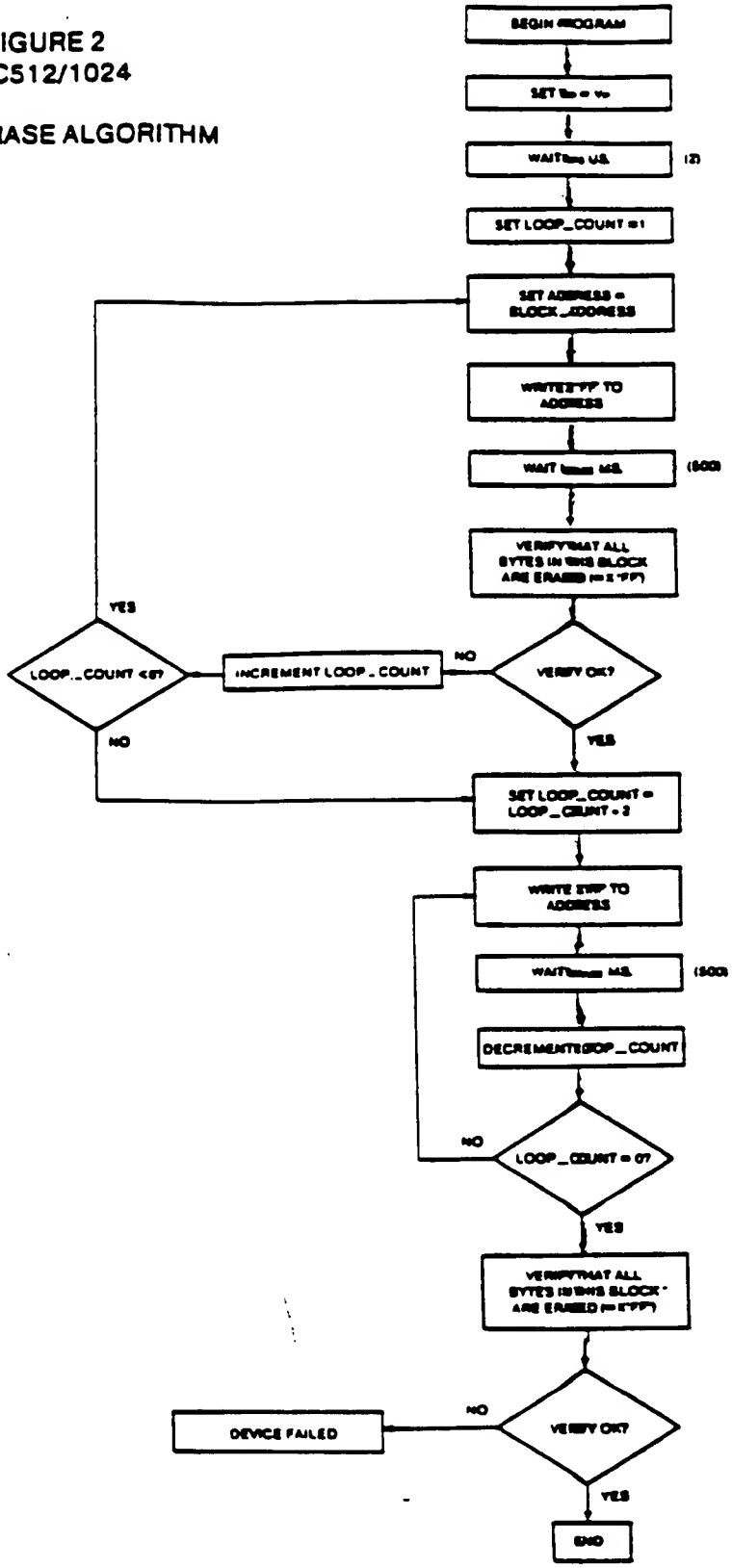


FIGURE 3
48C512/1024

CHIP ERASE ALGORITHM